REMARKS

Summary of the Amendment

Upon entry of the Amendment, the title of the invention and independent Claim 38 will have been amended. Claims 1-4, 8, 11, 28, 30-46 are currently pending.

Summary of the Official Action

In the present Office Action, the Examiner has objected to the title of the invention and rejected claims 1-4, 8, 28, 30-33, 35-43 and 45-46 over the art of record. Claims 11, 34 and 44 where objected to as being dependent upon a rejected base; *however, the Examiner did not reject claims 11, 34 and 44 over any art of record.* By the reply, which includes an amendment to the title and a traversal to the rejection with remarks, Applicant submits that proper and persuasive arguments have been presented which overcome the rejections. Therefore, the Applicant respectfully requests reconsideration of the outstanding Office Action and the allowance of the present application.

Objection to the Title of the Invention

The Examiner submits that the title of the invention, "Semiconductor Package Including Stacked Chips" is not descriptive. Applicant traverses the Examiner's contention that the title is not descriptive. In particular, the present invention discloses various embodiments of semiconductor packages which include stacked chips, and the title succinctly reflects this aspect of the invention. However, to expedite prosecution, Applicant has amended the title of the invention to "Semiconductor Package Including Stacked Chips With Aligned Input/Output Pads".

Traversal of Rejection Under 35 U.S.C. § 103(a)

Applicant traverses the rejection of Claims 1-4, 8, 28, 30-33, 35-43, and 45-46 under 35 U.S.C. § 103(a) as being unpatentable over Haung et al. (U.S. Patent No. 6,414,385) [hereinafter "HAUNG"] in view of Hung (U.S. Patent No. 6,476,474) [hereinafter "HUNG"].

The Examiner contends that HAUNG (see Figure 7) teaches a plurality of horizontal leads 326, a first chip having input/output pads, a second chip 304 having input/output pads electrically connected to a first side of the leads, and a packaged body formed of hardened encapsulating material 332 covering at least portions of the chips and at least a portion of the second side of the leads. The Examiner admits that HAUNG fails to explicitly show superimposed input/output pads.

The Examiner then cites HUNG as showing a dual-die package structure and method. The Examiner argues that HUNG shows superimposed input/output pads. Furthermore, the Examiner submits that it would have been obvious to one of ordinary skill in the art to use the purported superimposed input/output pads of HUNG with the device of HUANG for the purpose of providing a better electrical connection.

Applicant respectfully submits that the Examiner's rejection under 35 U.S.C. § 103(a) is inappropriate on several grounds, each of which is discussed below.

Base Claims 1 and 38:

Neither HUANG nor HUNG teach or suggest a second semiconductor chip *having central input/output pads*.

Independent Claim 1 recites, *inter alia*, a second semiconductor chip *having central input/output pads* and peripheral input/output pads. Independent Claim 38 recites, *inter alia*, a second semiconductor having a *plurality of central input/output pads* and a plurality of peripheral input/out pads. Applicant submits that HUANG and HUNG when viewed individually or considered in combination, fail to disclose or suggest the aforementioned features recited in base Claims 1 and 38.

HUANG teaches a first chip 310 and a second chip 304. The first chip 310 has exposed bonding pads 314 on the active surface 312a of the first chip 310. The second chip

304 is similarly configured to the first chip 310, the second chip 304 having exposed bonding pads 308 on the active surface 306a thereof. For each chip 310, 304, the bonding pads 314, 310 are located proximate to the outer edges thereof. However, neither the first chip 310 nor the second chip 304 has any central input/output pads.

HUNG teaches a first semiconductor die 100 and second semiconductor die 200. The first die 100 has a circuit surface 100a having a lined array of bond pads 110 one edge of the circuit surface 100a. Similarly, the second die 200 has a circuit surface 200a having a lined array of bond pads 210 on one edge of the circuit surface 200a. However, neither the first die 100 nor the second die 200 has any central input/output pads.

Applicant submits that none of the applied references teach or suggest when taken individually or in any proper combination, a second semiconductor chip *having central input/output pads* and peripheral input/output pads, as recited in base Claim 1. Furthermore, none of the applied references teach or suggest when taken individually or in any proper combination, a second semiconductor having a *plurality of central input/output pads* and a plurality of peripheral input/out pads, as recited in base Claim 38.

Accordingly, Applicant submits that no proper combination of the applied documents can render unpatentable the combination of features recited in at least Claims 1 and 38. Therefore, Applicant requests that the Examiner reconsider and withdraw the rejection of base Claims 1 and 38 under 35 U.S.C. § 103(a) and indicate that these claims are allowable over the art of record.

Further, Applicant submits that Claims 2-4, 8, 11 and 39-46 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. Therefore, Applicant requests that the Examiner reconsider and withdraw the rejection of Claims 2-4, 8, 11 and 39-46 under 35 U.S.C. § 103(a) and indicate that these claims are allowable over the art of record.

Neither HUANG nor HUNG teach or suggest *superimposed or aligned input/output pads*.

Independent Claim 1 recites, *inter alia*, *each of the central input/output pads superimposes and is electrically connected to a respective one of the input/output pads of the first semiconductor chip, and each of the peripheral input/output pads superimposes and is electrically connected to the first side of a respective one of the leads.*

Independent Claim 38 recites, *inter alia*, *each of the central input/output pads being aligned with electrically connected to a respective one of the input/output pads of the first semiconductor chip, with each of the peripheral input/output pads being aligned with and electrically connected to the first side of a respective one of the leads.* Applicant submits that HUANG and HUNG when viewed individually or considered in combination, fail to disclose or suggest the aforementioned features recited in base Claims 1 and 38.

The Examiner contends that HUNG specifically shows superimposed input/output pads. The Examiner's interpretation of HUNG is in error. As discussed previously, HUNG teaches a first semiconductor die 100 and second semiconductor die 200. The first die 100 has a circuit surface 100a having a lined array of bond pads 110 one edge thereof, and a non-circuit surface 100b. Similarly, the second die 200 has a circuit surface 200a having a lined array of bond pads 210 on one edge thereof, and a non-circuit surface 200b. HUNG further teaches stacking the first and second dies 100, 200 by adhering the circuit surface 100a of first die 100 to the circuit surface 200a of the second die 200 with an adhesive layer 220. *However, HUNG does not teach electrically connecting the first die 100 to the second die 200 via superimposed or aligned input/output pads disposed on circuit surface 100a and circuit surface 200a.* It appears the Examiner has mistakenly assumed that there is an electrical connection between the circuit surface 100a and circuit surface 200a, but this is not the case. If anything, it is quite clear that the adhesive layer 220 acts as an insulating layer between the circuit surface 100a and circuit surface 200a. In contradiction to the Examiner's argument, HUNG actually only teaches *offsetting* the lined array of bond pads 110 relative to the lined array of bond pads 210.

Furthermore, there is absolutely no teaching or suggestion in HUANG of the bonding pads 306b, 308, 314 *superimposing* or being *aligned with* the first surfaces 328a of the leads

326 (see Figure 7), or in HUNG of the bond pads 110, 210 *superimposing* or being *aligned with* any surface of the leads 310, 320 (see Figure 2F) .

Accordingly, Applicant submits that no proper combination of the applied documents can render unpatentable the combination of features recited in at least Claims 1 and 38. Therefore, Applicant requests that the Examiner reconsider and withdraw the rejection of base Claims 1 and 38 under 35 U.S.C. § 103(a) and indicate that these claims are allowable over the art of record.

Further, Applicant submits that Claims 2-4, 8, 11 and 39-46 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. Therefore, Applicant requests that the Examiner reconsider and withdraw the rejection of Claims 2-4, 8, 11 and 39-46 under 35 U.S.C. § 103(a) and indicate that these claims are allowable over the art of record.

Base Claim 28:

Neither HUANG nor HUNG teach or suggest *electrically connecting the input/output pads of the first semiconductor chip to respective ones of the input/output pads of the second semiconductor chip*, and placing input/output pads of one of the first and second semiconductor chips *over the first sides of the leads.*

Independent Claim 28 recites, *inter alia*, at least some of the input/output pads of the first semiconductor chip *face and are electrically connected to respective ones of the input/output pads of the second semiconductor chip by a first conductor*, and other input/output pads of one of the first and second semiconductor chips *are over the first sides of the leads and are each electrically connected to the first side of a respective one of the leads by a second conductor.* Applicant submits that HUANG and HUNG when viewed individually or considered in combination, fail to disclose or suggest the aforementioned features recited in base Claim 28.

As previously discussed, HUNG teaches a first semiconductor die 100 and second semiconductor die 200. The first die 100 has a circuit surface 100a having a lined array of

bond pads 110 one edge thereof, and a non-circuit surface 100b. Similarly, the second die 200 has a circuit surface 200a having a lined array of bond pads 210 on one edge thereof, and a non-circuit surface 200b. HUNG further teaches stacking the first and second dies 100, 200 by adhering the circuit surface 100a of first die 100 and the circuit surface 200a of the second die 200 with an adhesive layer 220. *However, HUNG does not teach electrically connecting the first die 100 to the second die 200 via facing input/output pads disposed on circuit surface 100a and circuit surface 200a.* It appears that the Examiner has mistakenly assumed that there is an electrical connection between the circuit surface 100a and circuit 200a, but this is not the case. It is quite clear that the adhesive layer 220 acts as an insulating layer between the circuit surface 100a and circuit surface 200a.

Furthermore, there is absolutely no teaching or suggestion in HUANG of the bonding pads 306b, 308, 314 being positioned *over* the first surfaces 328a of the leads 326 (see Figure 7), or in HUNG of the bond pads 110, 210 being positioned *over* any surface of the leads 310, 320 (see Figure 2F) .

Accordingly, Applicant submits that no proper combination of the applied documents can render unpatentable the combination of features recited in base Claim 28. Therefore, Applicant requests that the Examiner reconsider and withdraw the rejection of base Claim 28 under 35 U.S.C. § 103(a) and indicate that this claim is allowable over the art of record.

Further, Applicant submits that Claims 30-32 and 34-37 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. Therefore, Applicant requests that the Examiner reconsider and withdraw the rejection of Claims 30-32 and 34-37 under 35 U.S.C. § 103(a) and indicate that these claims are allowable over the art of record.

Acknowledgement of Allowable Subject Matter?

Claims 11, 34 and 44 where objected to as being dependent upon a rejected base; however, the Examiner did not reject Claims 11, 34 and 44 over any art of record. Applicant respectfully requests the Examiner to clarify his/her position as to whether Claims 11, 34 and

44 were intended to be cited as being allowable if presented in independent form that includes all the features of their base claim and any intervening claims.

CONCLUSION

Applicant respectfully submits that each and every pending claim of the present invention meets the requirements for patentability, and respectfully requests the Examiner to indicate the allowance thereof.

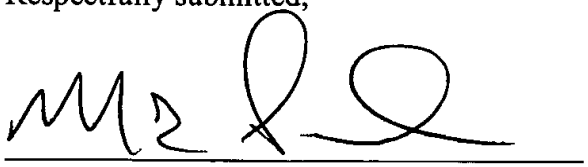
In view of the foregoing, it is submitted that none of the references of record, either taken alone or in any proper combination thereof, anticipate or render obvious the Applicant's invention as recited in Claims 1-4, 8, 11, 28, 30-30-46. The applied references have been discussed and distinguished, while significant claimed features of the present invention have been pointed out.

Accordingly, reconsideration of the outstanding Office Action and allowance of the present application and all the claims therein is respectfully requested and now believed to be appropriate.

Should there be any questions, the Examiner is invited to contact the undersigned at the below listed number.

If any additional fee is required, please charge Deposit Account Number 19-4330.

Respectfully submitted,

Date: 9/17/03 By: 

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